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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,227	09/03/2003	Bin Yu	H1486	4868

45114 7590 10/15/2004

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EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/653,227	YU ET AL.	
	Examiner	Art Unit	
	MARK V PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *September 3, 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the papers filed on September 3, 2003.

Claims 1-3, 6-12, 15, 16, 18 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by An et al. (United States Patent 6,800,885 – hereafter An).

With respect to independent claim 1, An discloses (see the entire patent, including the Figs. 19-24 disclosure) a semiconductor device comprising: an insulator 1920; a semiconductor fin 1930 formed on the insulator; a source region adjacent a first end of the fin formed on the insulator (note column 4, lines 35-38, for example); a drain region adjacent a second end of the fin formed on the insulator (note column 4, lines 35-38, for example); a first sidewall spacer 2010 formed adjacent a first side of the fin, the first sidewall spacer having a substantially triangular shaped cross-section; a second sidewall spacer 2020 formed adjacent a second side of the fin, the second sidewall spacer having a substantially triangular shaped cross-section; and a gate 2410 formed over the fin and the first and second sidewall spacers in a channel region of the semiconductor device. Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to dependent claim 2, An's first and second spacers cause a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers. Claim 2 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to dependent claim 3, An's first and second spacers slope away from the fin. Claim 3 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to dependent claim 6, An's first and second sidewall spacers are formed of polysilicon (see column 6, line 40, through column 7, line 12). Claim 6 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to dependent claim 7, An's gate electrode is formed of polysilicon (see column 6, line 40, through column 7, line 12). Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to independent claim 8, An discloses (see the entire patent, including the Figs. 19-24 disclosure) a method of manufacturing a semiconductor device, the method comprising: forming a fin structure 1930 on an insulator 1920; forming a first sidewall spacer 2010 adjacent a first side of the fin structure, the first sidewall spacer having a substantially triangular shaped cross-section; forming a second sidewall spacer 2020 adjacent a second side of the fin structure, the second sidewall spacer having a substantially triangular shaped cross-section; depositing a gate material layer 2410 over the fin structure, the first sidewall spacer, and the second sidewall spacer, the first and second sidewall spacers causing a gradual sloping of the gate material layer over the fin and the first and second sidewall spacers; and etching the gate material to form at least one gate for the semiconductor device (note column 4, lines 28-29, for example). Claim 8 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to dependent claim 9, the gradual sloping of An's gate material layer reduces micromasking effects during the etching of the gate material layer (note the

specification at paragraph [0030]). Claim 9 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to dependent claim 10, An's method further comprises forming a source region at a first end of the fin structure (note column 4, lines 35-38, for example). Claim 10 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to dependent claim 11, An's method further comprises forming a drain region at a second end of the fin structure (note column 4, lines 35-38, for example). Claim 11 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to dependent claim 12, An's first and second sidewall spacers comprise polysilicon (see column 6, line 40, through column 7, line 12). Claim 12 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to dependent claim 15, An's gate electrode comprises polysilicon (see column 6, line 40, through column 7, line 12). Claim 15 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to independent claim 16, An discloses (see the entire patent, including the Figs. 19-24 disclosure) a semiconductor device comprising: an insulator 1920; a semiconductor fin 1930 formed on the insulator; a source region connected to a first end of the fin and formed on the insulator (note column 4, lines 35-38, for example); a drain region connected to a second end of the fin and formed on the insulator (note column 4, lines 35-38, for example); a first sidewall spacer 2010 formed adjacent a first

side of the fin in a roughly triangular shape; a second sidewall spacer 2020 formed adjacent a second side of the fin in a roughly triangular shape; and a gate material layer 2410 formed over the fin, the first sidewall spacer, and the second sidewall spacer in a direction perpendicular to a direction of the fin, whereby the first and second sidewall spacers cause a topology of the gate material to smoothly transition over the fin and the first and second sidewall spacers. Claim 16 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to dependent claim 18, An's first and second sidewall spacers slope away from the fin. Claim 18 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

With respect to dependent claim 19, An's first and second sidewall spacers reduce micromasking effects during etching of a gate material to form the gate (note the specification at paragraph [0030]). Claim 19 is thus rejected under 35 U.S.C. 102(e) as being anticipated by An.

Claims 1-3, 6, 7, 16, 18 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Fried et al. (United States Patent 6,657,252 – already of record).

With respect to independent claim 1, Fried discloses (see the entire patent, including the Fig. 11 disclosure) a semiconductor device comprising: an insulator 99; a semiconductor fin 100 formed on the insulator; a source region adjacent a first end of the fin formed on the insulator (note column 6, lines 47-50, for example); a drain region adjacent a second end of the fin formed on the insulator (note column 6, lines 47-50, for

example); a first sidewall spacer 115 formed adjacent a first side of the fin, the first sidewall spacer having a substantially triangular shaped cross-section; a second sidewall spacer 115 formed adjacent a second side of the fin, the second sidewall spacer having a substantially triangular shaped cross-section; and a gate 120 formed over the fin and the first and second sidewall spacers in a channel region of the semiconductor device. Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fried.

With respect to dependent claim 2, Fried's first and second spacers cause a topology of the gate to smoothly transition over the fin and the first and second sidewall spacers. Claim 2 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fried.

With respect to dependent claim 3, Fried's first and second spacers slope away from the fin. Claim 3 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fried.

With respect to dependent claim 6, Fried's first and second sidewall spacers are formed of polysilicon (see column 5, lines 39-46). Claim 6 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fried.

With respect to dependent claim 7, Fried's gate electrode is formed of polysilicon (see column 6, lines 1-5). Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fried.

With respect to independent claim 16, Fried discloses (see the entire patent, including the Fig. 11 disclosure) a semiconductor device comprising: an insulator 99; a

semiconductor fin 100 formed on the insulator; a source region connected to a first end of the fin and formed on the insulator (note column 6, lines 47-50, for example); a drain region connected to a second end of the fin and formed on the insulator (note column 6, lines 47-50, for example); a first sidewall spacer 115 formed adjacent a first side of the fin in a roughly triangular shape; a second sidewall spacer 115 formed adjacent a second side of the fin in a roughly triangular shape; and a gate material layer 120 formed over the fin, the first sidewall spacer, and the second sidewall spacer in a direction perpendicular to a direction of the fin, whereby the first and second sidewall spacers cause a topology of the gate material layer to smoothly transition over the fin and the first and second sidewall spacers. Claim 16 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fried.

With respect to dependent claim 18, Fried's first and second sidewall spacers slope away from the fin. Claim 18 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fried.

With respect to dependent claim 19, Fried's first and second sidewall spacers reduce micromasking effects during etching of a gate material to form the gate (note the specification at paragraph [0030]). Claim 19 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fried.

Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over An et al. (United States Patent 6,800,885 – hereafter An) together with Dakshina-Murthy et al. (United States Patent 6,787,476 – hereafter Dakshina).

Claims 4 and 13 depend on independent claims 1 and 8, respectively, which are rejected under 35 U.S.C. 102(e) as being anticipated by An (see above). The above explanation of the rejection of claim 1 and 8 under 35 U.S.C. 102(e) as being anticipated by An is hereby incorporated by reference into this rejection of claims 4 and 13 under 35 U.S.C. 103(a) as being unpatentable over An together with Dakshina.

The difference, therefore, between claims 4/13 and An is claims 4/13 recite that the gate includes an electrode portion formed away from the fin (An does not have a plan view illustrating the gate away from the fin).

Dakshina teaches that a FinFET's gate conventionally includes an electrode portion formed away from the fin (see the Fig. 14B disclosure, for example).

It would have been obvious to one skilled in this art to form An's gate with an electrode portion away from the fin because Dakshina teaches that a FinFET's gate is conventionally provided with an electrode portion away from the fin.

Claims 4 and 13 are thus rejected under 35 U.S.C. 103(a) as being unpatentable over An together with Fried.

Claims 5, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over An et al. (United States Patent 6,800,885 – hereafter An) together with Lin (United States Patent 5,663,586).

Claims 5, 14 and 17 depend on independent claims 1, 8 and 16, respectively, which are rejected under 35 U.S.C. 102(e) as being anticipated by An (see above). The above explanation of the rejection of claim 1, 8 and 16 under 35 U.S.C. 102(e) as being

anticipated by An is hereby incorporated by reference into this rejection of claims 5, 14 and 17 under 35 U.S.C. 103(a) as being unpatentable over An together with Lin.

The difference, therefore, between claims 5/14/17 and An is claims 5/14/17 recite that the sidewall spacers are formed with a width of about 150 Å to about 1000 Å (An does not disclose the width of its sidewall spacers).

Lin teaches that polysilicon sidewall spacers are conventionally formed with a width of 200 Å to 1000 Å (see column 4, lines 39-46).

It would have been obvious to one skilled in this art to form An's polysilicon sidewall spacers with a width of about 150 Å to about 1000 Å because Lin teaches that polysilicon sidewall spacers are conventionally formed that thick.

Claims 5, 14 and 17 are thus rejected under 35 U.S.C. 103(a) as being unpatentable over An together with Lin.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner